

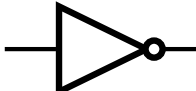







Existing logic gates

Type	Symbol	How it works	Truth table																		
AND		Only if both inputs are 1 is the output 1. Otherwise, the output is 0.	<table border="1"> <thead> <tr> <th colspan="2">Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Input		Output	A	B		0	0	0	0	1	0	1	0	0	1	1	1
Input		Output																			
A	B																				
0	0	0																			
0	1	0																			
1	0	0																			
1	1	1																			
OR		Only if both inputs are 0 is the output 0.	<table border="1"> <thead> <tr> <th colspan="2">Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Input		Output	A	B		0	0	0	0	1	1	1	0	1	1	1	1
Input		Output																			
A	B																				
0	0	0																			
0	1	1																			
1	0	1																			
1	1	1																			
NOT		If the input is 1, the output is 0. If the input is 0, the output is 1.	<table border="1"> <thead> <tr> <th>Input</th> <th>Output</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> </tr> </tbody> </table>	Input	Output	0	1	1	0												
Input	Output																				
0	1																				
1	0																				
NAND		Only if both inputs are 1 is the output 0. Otherwise, the output is 1.	<table border="1"> <thead> <tr> <th colspan="2">Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Input		Output	A	B		0	0	1	0	1	1	1	0	1	1	1	0
Input		Output																			
A	B																				
0	0	1																			
0	1	1																			
1	0	1																			
1	1	0																			
NOR		Only if both inputs are 0 is the output 1.	<table border="1"> <thead> <tr> <th colspan="2">Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Input		Output	A	B		0	0	1	0	1	0	1	0	0	1	1	0
Input		Output																			
A	B																				
0	0	1																			
0	1	0																			
1	0	0																			
1	1	0																			
XOR		Only if one of the inputs (but not both) is 1, the output is 1. Otherwise, the output is 0.	<table border="1"> <thead> <tr> <th colspan="2">Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	Input		Output	A	B		0	0	0	0	1	1	1	0	1	1	1	0
Input		Output																			
A	B																				
0	0	0																			
0	1	1																			
1	0	1																			
1	1	0																			
XNOR		Only if both inputs are the same (two 0s or two 1s) is the output 1.	<table border="1"> <thead> <tr> <th colspan="2">Input</th> <th>Output</th> </tr> <tr> <th>A</th> <th>B</th> <th></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> </tr> </tbody> </table>	Input		Output	A	B		0	0	1	0	1	0	1	0	0	1	1	1
Input		Output																			
A	B																				
0	0	1																			
0	1	0																			
1	0	0																			
1	1	1																			

Proposed additional logic gate

BUT		Stops the functioning of the circuit and raises a concern.	N/A
-----	---	--	-----